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Igarashi, Brian; Christensen, Tage Emil; Larsen, Ebbe Hyldahl; Olsen, Niels Boye; Pedersen, Ib Høst; Rasmussen, Torben Steen; Dyre, J. C.

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An impedance-measurement setup optimized for measuring relaxations of glass-forming liquids

Brian Igarashi, Tage Christensen, Ebbe H. Larsen, Niels Boye Olsen, Ib H. Pedersen, Torben Rasmussen, and Jeppe C. Dyre
DNRF Centre "Glass and Time," IMFUFA, Department of Sciences, Roskilde University, Postbox 260, DK-4000 Roskilde, Denmark

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An electronics system has been assembled to measure frequency-dependent response functions of glass-forming liquids in the extremely viscous state approaching the glass transition. We determine response functions such as dielectric permittivity and shear and bulk moduli by measuring electrical impedances of liquid-filled transducers, and this technique requires frequency generators capable of producing signals that are reproducible over the span of several days or even several weeks. To this end, we have constructed a frequency generator that produces low-frequency (1 mHz–100 Hz) sinusoidal signals with voltages that are reproducible within 10 ppm. Two factors that partly account for this precision are that signals originate from voltages stored in a look-up table and that only coil-less filters are used in this unit, which significantly reduces fluctuations of output caused by changes of temperatures of circuits. This generator also includes a special triggering facility that makes it possible to measure up to 512 voltages per cycle that are spaced apart at uniform phase intervals. Fourier transformations of such data yield precise determinations of complex amplitudes of voltages and currents applied to a transducer, which ultimately allows us to determine electrical impedances of transducers with a reproducibility error that is only a few parts per hundred thousand. This equipment is used in tandem with a commercial *LCR* meter and/or impedance analyzer that give(s) impedance measurements at higher frequencies, up to 1 MHz. The experimental setup allows measurements of the transducer impedance over nine decades of frequency within a single run. © *2008 American Institute of Physics.* [DOI: 10.1063/1.2906401]

I. INTRODUCTION

Any liquid may be brought into the glassy state if rapidly cooled enough to avoid crystallization. Since glass is formed from a liquid, a better understanding of glass properties is expected to come from a better understanding of the highly viscous liquid phase preceding glass formation.[1] A characteristic feature of highly viscous liquids approaching the glass transition is their very long relaxation times. The relaxation time quickly increases upon cooling, and the glass transition is the falling out of equilibrium taking place when the liquid relaxation time exceeds the laboratory time scale, thus inhibiting the liquid from coming to equilibrium. These extremely long relaxation times imply that well-known thermodynamic linear response properties such as specific heat and expansion coefficients become frequency dependent at low frequencies (millihertz to kilohertz, depending on temperature). Linear thermoviscoelasticity deals with frequency dependences of thermodynamic properties and their couplings to frequency-dependent mechanical properties. It is understood that, in principle, only infinitesimal perturbations are applied, thus ensuring linearity.

We are presently developing techniques that convert the problem of measuring certain linear frequency-dependent response functions into measuring frequency-dependent electrical impedances. More specifically, we measure complex frequency-dependent electrical capacitances of liquid-filled transducers. The dielectric permittivity of a liquid is measured by depositing a small quantity between plates of a dielectric cell and then measuring electrical capacitance of the cell. This is a standard technique, but perhaps less well known is that mechanical properties (bulk and shear moduli) of liquids also can be detected by measuring capacitances of liquid-filled piezoceramic transducers.[2,3] The transducers possess extra (real) capacitance originating from the piezoelectric nature of the material, and when a liquid is in contact with the transducer, it inhibits this motion and, thereby, partially cancels the capacitance due to the piezoelectric effect. We thereby determine the stiffness or shear modulus of a liquid by measuring reduction of the electrical capacitance of a piezoceramic transducer that is caused by the liquid's presence.

In order to accurately measure the reduction of capacitance, we need to replicate experimental conditions for the two cases of when the transducer is empty and when it is filled with liquid. For example, we must be able to set the temperature in a repeatable fashion, and, in order to accomplish this, we have built a cryostat and temperature control system that is described in a companion article.[4] It also is essential to apply the same voltage to a transducer when it is empty and when filled. The custom-built frequency generator described in the present article is designed to meet this requirement. Below, we shall explain details of steps taken to create a highly reproducible signal. In addition, we shall describe a special triggering facility that is incorporated in the

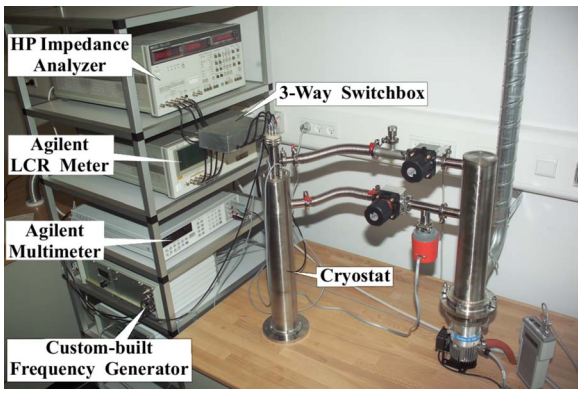

FIG. 1. (Color online) An overview of equipment for measuring the electrical impedance or capacitance of a transducer mounted in a cryostat.

unit to make it possible to measure multiple voltages per cycle that are spaced apart at uniform phase intervals. Fourier transformations of such data yield precise determinations of complex amplitudes of voltages and currents applied to a transducer, which allows us to determine electrical impedances of transducers with a reproducibility error that is only a few parts per hundred thousand.

II. COMMERCIAL EQUIPMENT USED TO MEASURE ELECTRICAL CAPACITANCES OF TRANSDUCERS

Depending upon frequency, different commercial and custom-built instruments are used to measure electrical impedance or capacitance of a transducer (Fig. 1). A precision *LCR* meter (Agilent 4284A with frequency range of 20 Hz–1 MHz) and an impedance analyzer (Hewlett-Packard 4192A with frequency range of 5 Hz–13 MHz) are available for measurements above 100 Hz. Since the *LCR* meter performs measurements with higher accuracy (discussed in detail below), we typically rely upon this unit to acquire measurements from 100 Hz to frequencies on the order of 10 kHz, whereupon the relative sparsity of frequencies preprogrammed in the unit compels us to switch to the impedance analyzer. (One improvement currently being undertaken is replacement of the *LCR* meter with an updated model (Agilent E4980A), which has more frequencies available in the upper frequency ranges and, thus, eliminates the need for the impedance analyzer.) A custom-built frequency generator (described below in Sec. III) is used in tandem with an $8\frac{1}{2}$-digit multimeter (Agilent 3458A) to perform measurements from 1 mHz to 100 Hz. A software-controlled switchbox automatically connects a transducer to the various instruments in succession, allowing us to measure the capacitance of a transducer over nine decades of frequencies within a single run.

An idealized scheme for measuring electrical impedance of a transducer is shown in Fig. 2. A perfect oscillator establishes vector (complex) voltage V_x across a transducer, and, if vector current I_x through the transducer is measured using a perfect ammeter, electrical impedance Z_x equals the ratio, V_x/I_x. For transducers that are largely capacitivelike in nature, Z_x is most appropriately expressed in terms of complex capacitance $C_x=C'+iC''$ and angular frequency ω: $Z_x=(i\omega C_x)^{-1}$. Imaginary component C'' arises from energy

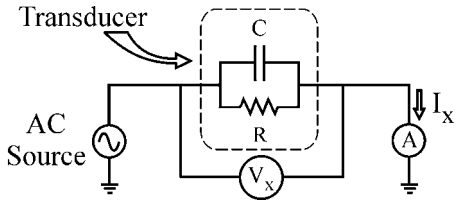

FIG. 2. Idealized setup for measuring the electrical impedance of a transducer. Voltage V_x across the transducer is measured by a perfect vector voltmeter, and current I_x is measured by a perfect vector ammeter. The parallel R and C lumped elements are appropriate for modeling capacitivelike transducers. (In general, R and C are frequency dependent.)

loss in the transducer, and it equals $-D\,C'$, where D is the dissipation factor or loss tangent (often much less than 1). (Throughout this section, we assume that the transducer is capacitivelike, meaning that C' is positive; however, if the transducer should become inductivelike for a certain range of frequencies, C' becomes negative, and sign changes may be necessary in certain expressions of this section.) For simplicity's sake, the source of loss is represented by shunt resistor R in the figure (perhaps accounting for electrical loss due to leakage currents; more sophisticated circuits are required to model losses associated with relaxation processes in liquids). In terms of components of the equivalent circuit, $D=(\omega RC)^{-1}$, $C'=C$ and $C''=-(\omega R)^{-1}$. As a specific example, piezoceramic transducers used in our studies typically have values of C that are on the order of 10 nF and values of D and R that vary with frequency (for example, at 0.01 Hz, the orders of magnitude of D and R are 0.01 and 10^9 or 10^{10} Ω, respectively, but, at 10 kHz, they are of order 0.001 and 10^5 or $10^6\Omega$). As a side note, it is often convenient to analyze the parallel resistor-capacitor circuit in terms of admittance $Y_x=1/Z_x=G+iB$. Conductance G equals $1/R$, susceptance B equals ωC, and dissipation factor D equals G/B. The phase angle of Y_x (negative of the phase angle of Z_x) is $\arctan(D^{-1})$.

Impedance measurements performed by the *LCR* meter and impedance analyzer are carried out by using an autobalancing bridge.[5,6] The working principles behind this circuit are illustrated in Fig. 3. The ac source in this figure has an amplitude of 1 V. Impedance Z_x of the transducer is inferred from "balancing" it against a known load, resistor R_r. When no current flows through the null detector ($I_d=0$), voltage V_L of low point L on the diagram becomes 0 V, which implies that voltage V_H of high point H equals the voltage drop across the transducer. Since null current through the detector

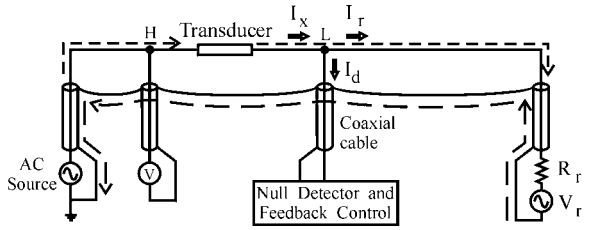

FIG. 3. Simplified model of an autobalancing bridge. The idealized V_r oscillator is assumed to have the same frequency as the ac source. The amplitude of the ac source is 1 V.

implies that current I_r through the resistor matches current I_x through the transducer, we have $V_H/Z_x=-V_r/R_r$ (the function of the ammeter in Fig. 2 is fulfilled by the combination of the V_r oscillator and R_r resistor) or $Z_x=(V_H/-V_r)R_r$. The bridge is balanced by adjusting the amplitude and phase of the V_r oscillator so that V_L equals zero, with corrections being automatically implemented through feedback control connected to the null detector.

To decrease errors caused by stray impedances in cable leads, the transducer is hooked up to the *LCR* meter and impedance analyzer in a four-terminal pair configuration. Four coaxial cables are required with their outer shields spliced together, ideally at points near the transducer. Negligible current flows into the cable connecting point H to the vector voltmeter, and, when the bridge is balanced, no current flows into the cable connecting point L to the null detector. Current is almost completely confined to flowing in the cable connected to the ac source and the cable connecting point L to resistor R_r. Most notably, current returns to the ac source along the outer shielding of these two cables. This has the effect of reducing self-inductance of the cables and mutual inductance between them, for exterior magnetic fields created from currents flowing in the inner conductors are canceled by fields created from shield currents flowing in the opposite direction.[7] It should be pointed out that the four-terminal pair configuration also offers advantages of an ordinary four-point measurement of impedance, where separate pairs of electrodes are used to power the transducer and sense the voltage drop across it. Since the voltage-sensing electrodes do not carry current, the voltage reading is not influenced by stray series resistance or inductance or shunt capacitance in the cables of the electrodes.

In spite of these preventive measures taken to avoid interference from stray impedances, these effects cannot be entirely eliminated. For example, although series inductance is suppressed to a large degree by the four-terminal pair configuration, some residual inductance is always introduced by short lengths of unshielded wires connecting coaxial cables to the transducer. It is necessary to identify these stray impedances and then accordingly process measurements to compensate for their effects. We characterize stray impedance effects by first replacing the transducer with a capacitor of known capacitance C_K (we use the same capacitor for calibrating the multimeter bridge circuit described in Sec. III below) and then performing an impedance measurement using the impedance analyzer. The capacitor is mounted in a cryostat under vacuum and its temperature is held at 220 K, which is within the range of typical temperatures at which we conduct measurements on transducers. It is observed that stray impedance effects become noticeable at high frequencies, for example, causing a 0.1% deviation of capacitance at around 100 kHz. Frequency dependence of the effects can be modeled as arising from a resistance R_s and inductance L_s lying in series with C_K, which indicates that the stray impedances may indeed be due to bare wire connections in the setup. For the case of C_K given by a 20 nF capacitor, the complex capacitance C_x of the total load may be fit to the expression, $1/C_x \cong (1/C_K)-\omega^2 L_s+i\omega R_s$, with $L_s=47.4$ nH and $R_s=0.053\ \Omega$. This result then supplies us with a technique by which we can compensate for effects of stray impedances: we merely need to subtract the last two terms from measurements of $1/C_x$.

Both the *LCR* meter and the impedance analyzer are controlled by a PC running a MATLAB (Ref. 8) program on a Windows platform. All communications with the PC occur through a general purpose interface bus line. The *LCR* meter is programed to measure the parallel capacitance (C in Fig. 2) and dissipation factor D of the load over a range of preset calibration frequencies. For frequencies above 100 Hz, there are ten available frequencies in each decade, and the accuracy of frequencies is $\pm 0.01\%$. For measurements of a capacitance on the order of 10 nF at frequencies less than 100 kHz and with a "long" integration time (where data acquisition time is approximately 1 s), specifications of the instruments indicate that the relative accuracies (taking into account stability, linearity, and repeatability) of C and D are $\pm 0.05\%$ and ± 0.0005, respectively. If calibration accuracies are taken into account, too, absolute accuracies of C and D are $\pm(0.08$ to $0.10)\%$ and $\pm(0.0006$ to $0.0008)$, respectively.

When using the impedance analyzer, one can perform measurements at more frequencies, but with somewhat less accuracy. There is the option of logarithmically sweeping through a range of frequencies—with 20 frequencies available in each decade—or linearly sweeping through frequencies with step size specified by the user. The accuracy of frequencies is ± 50 ppm. For frequencies up to 1 MHz, the accuracy of the ac source (with amplitude set to 1 V) of the autobalancing bridge is ± 0.06 V. The unit is programed to measure conductance G and susceptance B of the load, which gives complex capacitance, $C_x=B/\omega-iG/\omega$. For piezoceramic transducers with values of C that are about 10 nF and for frequencies between 10 kHz and 1 MHz, accuracies of derived values of C and D $(=G/B)$ are $\pm 0.1\%$ and ± 0.001, respectively.

Figure 4 shows results of a test of the limits of the reproducibility error of the *LCR* meter. Two capacitors connected in parallel are mounted in the main cryostat and the temperature is lowered to 220 K to reduce electrical loss in the capacitors. Histograms in the figure show the distribution of three days' measurements performed with an excitation frequency of 100 Hz. (The non-Gaussian shape of the distributions indicates that the average drifts with time. This drifting perhaps reflects sensitivity of circuitry in the *LCR* meter to variations in laboratory room temperature (according to instrument specifications, temperature coefficients of real and imaginary parts of the capacitance readings may be as large as 0.61 pF/°C) and is not due to changing temperature of the capacitors since temperature dependence of their capacitance is -2 pF/°C and, as pointed out in Ref. 4, the main cryostat maintains their temperature within a few millikelvins) The mean value of measurements of the real part of capacitance is $C'=24.56$ nF, and the standard deviation of measurements is $\delta C'+i\delta C''=0.40+i0.24$ pF, which implies that reproducibility error of the real part of the capacitance is approximately $\delta C'/C'=16$ ppm and reproducibility error of dissipation factor D is approximately $\delta C''/C'=10$ ppm. These uncertainties are an order of magnitude smaller than

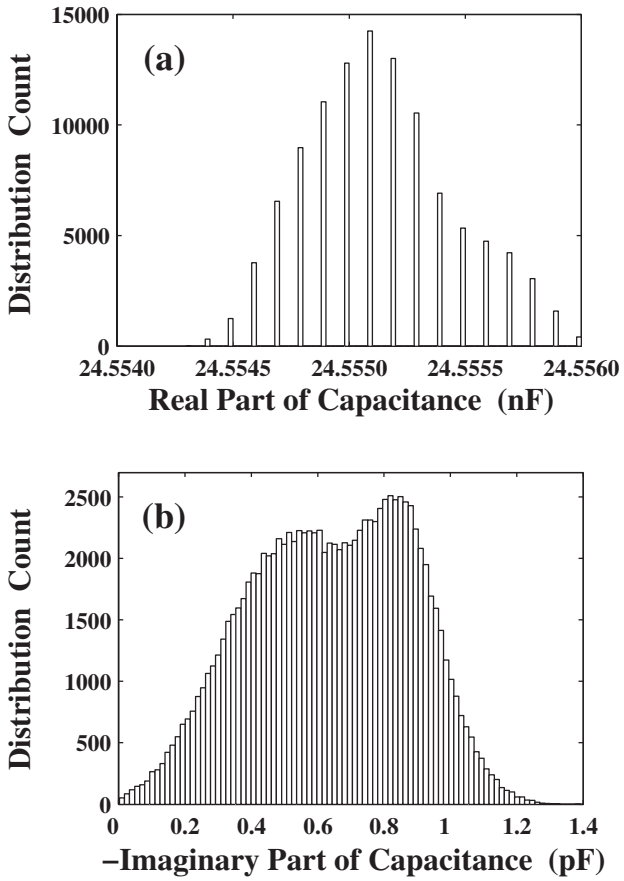

FIG. 4. Sample distributions of (a) real and (b) imaginary parts of measurements of capacitance using the *LCR* meter.

the accuracies cited above, which are given by the manufacturer's specifications and likely are proper estimates of reproducibility errors of measurements taken over the course of many months.

III. USE OF A CUSTOM-BUILT FREQUENCY GENERATOR TO MEASURE ELECTRICAL CAPACITANCES

When a custom-built frequency generator and multimeter are used to measure impedance, voltage V_x across the transducer and current I_x through the transducer are not measured directly but, rather, inferred through voltages measured in a potential divider arrangement [Fig. 5(a)]. With the generator supplying voltage V_{gen} (of amplitude 1.25 or 10 V) and a multimeter measuring voltage V_{in} across known dummy load Z_0 (which incorporates the high input impedance of the multimeter), V_x equals $V_{\mathrm{gen}}-V_{\mathrm{in}}$ and I_x equals V_{in}/Z_0. Taking the ratio of these two expressions to obtain transducer impedance Z_x, we find

$$Z_x = Z_0\left(\frac{V_{\mathrm{gen}}}{V_{\mathrm{in}}} - 1\right). \tag{1}$$

In order to maximize sensitivity of voltage V_{in} $[=V_{\mathrm{gen}}Z_0/(Z_x+Z_0)]$ to changes in transducer impedance Z_x (that is, maximize derivative $\partial V_{\mathrm{in}}/\partial Z_x$), Z_0 should match Z_x. Since this is the same criterion used to balance the original version of the Wheatstone bridge, we refer to this potential

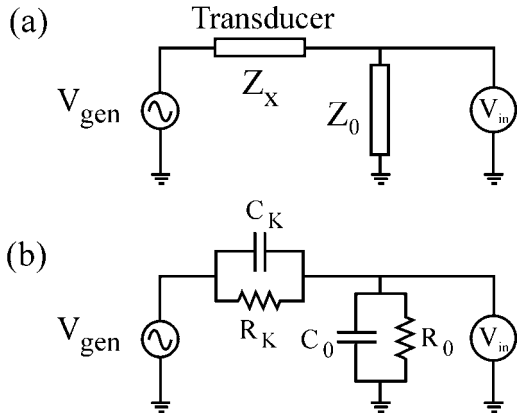

FIG. 5. Technique of measuring impedance of a transducer by using the custom-built frequency generator and commercial multimeter. (a) Bridge circuit for measuring the electrical impedance Z_x of a transducer using a custom-built frequency generator (supplying voltage V_{gen}) and a commercial multimeter (measuring voltage V_{in}). To maximize sensitivity of measurements, dummy impedance Z_0 is chosen to be close to Z_x. (Z_0 incorporates input impedance of the multimeter, which is greater than 10 GΩ) (b) Setup for determining values of dummy capacitor C_0 and resistor R_0 in terms of known values of capacitance C_K and resistance R_K. A parallel arrangement of a capacitor and a resistor is appropriate for modeling the impedance of a capacitivelike transducer.

divider arrangement as a "bridge circuit" (more precisely, it is one ratio arm of a Wheatstone bridge).

In order for the dummy load to resemble a capacitivelike transducer, we construct it out of a capacitor C_0 connected in parallel with resistor R_0 [shown in Fig. 5(b)], similar to the lumped-element model of the transducer (Fig. 2). As indicated above, piezoceramic transducers have values of C that are on the order of 10 nF and, for the range of frequencies issued by the custom-built frequency generator, R is at least 10^8 Ω. C_0 is chosen to be close to the real part of the capacitance of the particular type of transducer being measured, but, since the dummy load is not sensitive to the resistor value, we let R_0 be 10^8 or 10^9 Ω for all transducers. One practical constraint we are heedful of, though, is that R_0 should not be too large since this resistor serves the function of bleeding off charge buildup on the capacitor.

Nominal values of C_0 and R_0 are not precise enough to be used in Eq. (1), and these two parameters must be determined from a calibration procedure. This is done by replacing the transducer in Fig. 5(a) with a known capacitor C_K and then performing a measurement of the bridge circuit, with the dummy load now treated as an unknown [Fig. 5(b)]. To obtain high-resolution voltage readings during this calibration run, the amplitude of the generator output is set to 10 V (in contrast to Eq. (1), where, during transducer measurements, the amplitude may be 1.25 V). Rewriting Eq. (1) to isolate terms we are trying to ascertain, we derive

$$\frac{1}{Z_0} = i\omega C_0 + \frac{1}{R_0} = \left(i\omega C_K + \frac{1}{R_K}\right)\left(\frac{V_{\mathrm{gen}}}{V_{\mathrm{in}}} - 1\right). \tag{2}$$

The most important unknown, C_0, can be determined from the imaginary part of the expression on the right-hand side of this equation. Resistance R_K, representing the pathway of

leakage current in capacitor C_K, has a high order of magnitude, particularly since the calibration procedure is run with the capacitor placed in an evacuated cryostat at a temperature of 220 K in an effort to minimize losses. Estimates of R_K may require adjustment to obtain values of C_0 that are largely frequency independent, as they are expected to be.

The frequency generator can output 16 preset frequencies (logarithmically evenly spaced) in each decade between 1 mHz and 100 Hz (see Sec. IV D for details). Values of Z_0 are determined at each of these frequencies. The amplitude of generator voltage V_{gen} is also measured during the calibration procedure and is tabulated at each frequency. Once these values of Z_0 and V_{gen} are available to us, we can then proceed to ascertain impedance Z_x of a transducer mounted in the cryostat. We separately measure voltage V_{in} in the bridge circuit and then substitute values of Z_0, V_{gen}, and V_{in} into Eq. (1) to calculate impedance Z_x (expressed as complex capacitance C_x) at each frequency. Data-collection procedures do take into account start-up transients that are introduced into the signal when the generator switches frequency (transients are caused by the sudden shift in frequency, not by a shift in voltage): the generator is instructed to cycle through three or four times to allow transients to decay away before measurements of V_{gen} or V_{in} are accepted. As described in detail in Sec. IV E below, complex amplitudes of voltages V_{gen} and V_{in} are determined by measuring voltages at uniform phase intervals within each cycle and then performing a Fourier transform of this set of voltages. To ensure that we measure voltages that are evenly spaced apart in phase, a special triggering facility that precisely controls timing of voltage measurements by the multimeter has been incorporated in the design of the frequency generator (see Sec. IV for details).

Figure 6 reveals the reproducibility errors of values of V_{gen} that are measured with the aid of the special triggering facility. Histograms in the figure show distributions of amplitude and phase of a 1 Hz sinusoid that are acquired in 1 day of continuous measurements. The mean value of V_{gen} is approximately 1.25 V, and widths of distributions indicate that the relative reproducibility error $\delta V_{\text{gen}}/V_{\text{gen}}$ of the output voltage is on the order of $(1+i)$ ppm. As in Fig. 4, the non-Gaussian shape of the distribution of the signal amplitude may be attributed to drifting of the output that is likely caused by changes of temperature of the output circuitry of the frequency generator or the temperature of components in the multimeter. (According to instrument specifications, the temperature coefficient of the voltage reading by the multimeter may be as large as 0.6 ppm/ °C.) When measurements are repeated over a longer period of time (over a week), the reproducibility error is somewhat larger: $\delta V_{\text{gen}} = (10+i1.2)\ \mu\text{V}$ and $\delta V_{\text{gen}}/V_{\text{gen}} \cong (8+i)$ ppm. After 6 or 7 months, V_{gen} changes by tens of microvolts (both real and imaginary parts) and $\delta V_{\text{gen}}/V_{\text{gen}}$ is tens of ppm.

Figure 7 shows the results of a test of the limits of the reproducibility error of voltage V_{in}. We measure V_{in} in the bridge circuit of Fig. 5 with the transducer replaced by the same two capacitors used to test the *LCR* meter (they are mounted in the main cryostat with the temperature held at 220 K). Histograms in the figure show the distribution of 7 h of continuous measurements. Similar to the above estimate

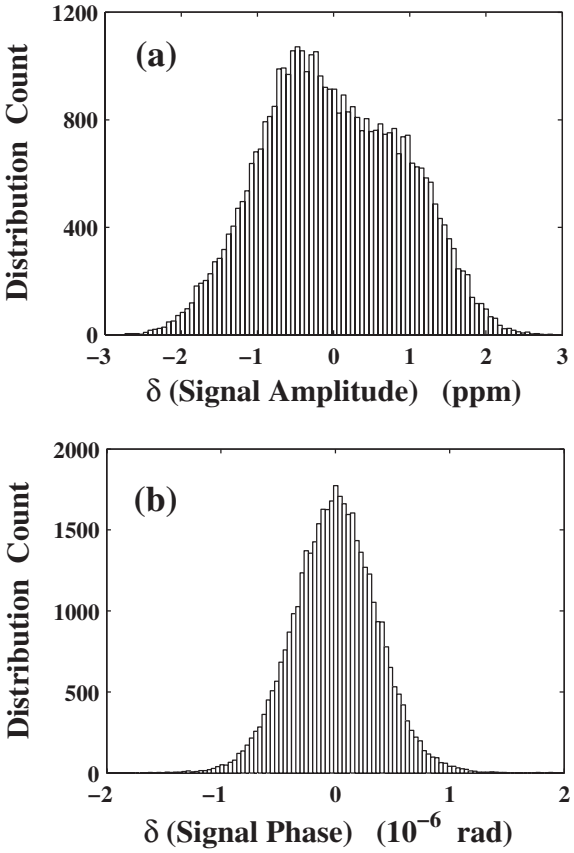

FIG. 6. Sample distributions of (a) amplitude and (b) phase of output voltage V_{gen} of the custom-built frequency generator. Average amplitude is 1.257 29 V and average phase is $3.742\,54 \times 10^{-4}$ rad.

of $\delta V_{\text{gen}}/V_{\text{gen}}$ for one day of measurements, the reproducibility error $\delta V_{\text{in}}/V_{\text{in}}$ is on the order of $(1+i)$ ppm, which is not surprising considering V_{in} is proportional to V_{gen} in the bridge circuit. Similar to V_{gen}, when measurements are repeated over a longer period of time (about three days), the reproducibility error is somewhat larger: $\delta V_{\text{in}} = 10+i9.0\ \mu\text{V}$ and $\delta V_{\text{in}}/V_{\text{in}} \cong 11+i10$ ppm.

Given these magnitudes of voltage errors, we can now calculate the reproducibility error of capacitances yielded by Eq. (1). If we assume that fluctuations of V_{gen} and V_{in} are uncorrelated (valid as a first approximation since V_{gen} and V_{in} are not simultaneously measured), the relative variance of capacitance C_x can be calculated from the following formula, which derives from treating propagating errors in standard fashion:[9]

$$\frac{\delta C_x}{C_x} = \left(1 + \frac{C_x}{C_0^*}\right)\sqrt{\left(\frac{\delta V_{\text{gen}}}{V_{\text{gen}}}\right)^2 + \left(\frac{\delta V_{\text{in}}}{V_{\text{in}}}\right)^2}. \tag{3}$$

The radical factor on the right-hand side derives from the relative error in $V_{\text{gen}}/V_{\text{in}}$, and, since these two voltage amplitudes are complex, the squared terms in Eq. (3) are treated as complex, too. Imaginary parts of the estimates of $\delta C_x/C_x$ mainly result from imaginary parts of δV_{gen} and δV_{in}. Here, C_x is the mean total capacitance of the capacitors held at 220 K (again, approximately 24.56 nF) and C_0^* is the equivalent complex capacitance of impedance Z_0 (10.321 nF$-i$164 pF). This value of C_0^* is measured at 1 Hz, the same frequency at which C_x and the voltages are mea-

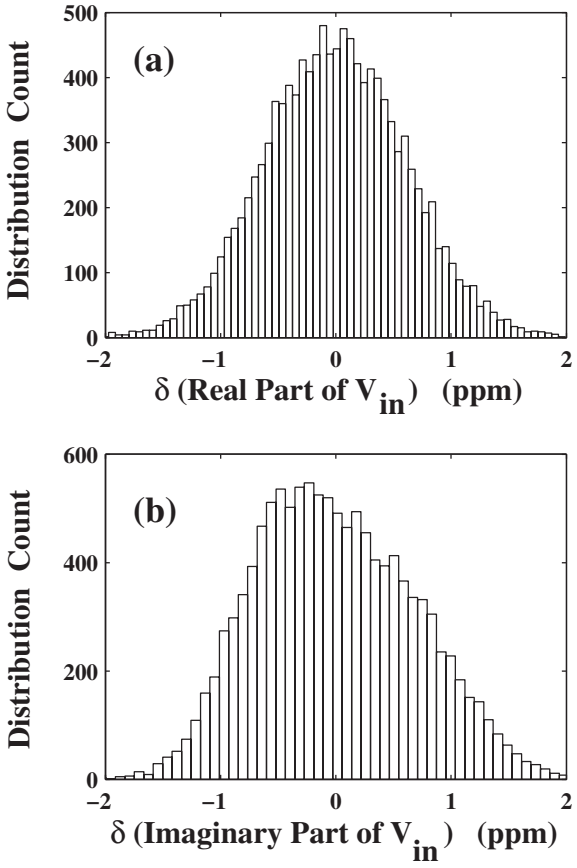

FIG. 7. Sample distributions of (a) real and (b) imaginary parts of the amplitude of voltage V_{in} in the bridge circuit of Fig. 5. The average value of V_{in} in this data set is $(0.874\,787+i4.792\,81\times10^{-3})$ V.

sured. The real part is given by capacitor C_0 in Fig. 5(b), and, since the capacitor inserted here is of a NPO type, which is recognized to be impervious to temperature changes and should show little aging effects, the real part should be a stable value. The imaginary part changes by only a fraction of a picofarad every six months. Consequently, if the time span of measurements does not exceed one or two weeks, fluctuations of C_0^* may be regarded as negligible, and, to first approximation, C_0^* is treated as a constant in Eq. (3). Substituting in above estimates of reproducibility errors of voltages, we calculate that $\delta C_x/C_x$ is around $5(1+i)$ ppm in the best case scenario where temperatures of critical electronic components in the box generator and multimeter are steady (usually occurring over a time span of a day or less). The reproducibility error of dissipation factor D is approximately $\delta C''/C'=5$ ppm (using $C_x=C''+iC''$). We note that these performance characteristics are slightly better than those observed with the *LCR* meter (see comments above about Fig. 4); however, for the more typical case where measurements are taken over several days and temperatures vary by a few degrees, $\delta C_x/C_x$ is approximately $40+i30$ ppm and δD is approximately 30 ppm. These errors are two to three times larger than those given by the *LCR* meter. We are currently investigating options for stabilizing temperatures of critical circuits to maintain the 5 ppm levels of reproducibility errors over longer periods of time (see comments in Sec. V).

FIG. 8. (Color online) Circuit boards containing components for the custom-built frequency generator.

IV. DETAILS OF CONSTRUCTION AND OPERATION OF THE CUSTOM-BUILT FREQUENCY GENERATOR

This section describes the custom-built unit (Fig. 8) that digitally generates low-frequency sinusoidal signals. The operating principle employed here is straightforward: sinusoidal signals are generated by outputting voltages that are stored in memory chips, and frequency is varied by varying the rate at which these voltages are outputted. For the working frequency range of this instrument (1 mHz–1 kHz), this technique works well, and it provides a couple of advantages. One, electronic circuits are relatively simple and economical to build. Two, the fact that signals originate from voltages stored in a look-up table promotes reproducibility of signals. In fact, final output voltages of the unit are reproducible with a variation of only parts per million. Part of this precision may be attributed to the fact that circuitry has been designed so that functionings of critical components do not vary much when the operating temperature fluctuates. For example, filters in this unit (for smoothing out steps that inevitably appear in digitally generated signals) do not use coils, which tend to significantly depend upon temperature (see the description of the filters in Sec. IV A).

Another distinctive feature of this generator is that it has a triggering facility that can issue multiple synchronizing trigger signals throughout each cycle, not solely at the beginning of a cycle, as is customary with commercial units. The trigger signals can be used to synchronize measuring instruments with the output of the generator, and, in our setup, we use an $8\frac{1}{2}$-digit multimeter in conjunction with the generator to measure the electrical impedance of a transducer. The multiple trigger signals (up to 512) offered each cycle afford the option of utilizing the precise time base of the generator to control timing of measurements by the multimeter. As a result of this precise timing and the fact that voltages of signals are highly reproducible, we are able to determine impedances of transducers with high precision. As shown above in Sec. III, depending upon how stable the laboratory room temperature is, the reproducibility error of our impedance measurements has a 1–10 ppm order of magnitude.

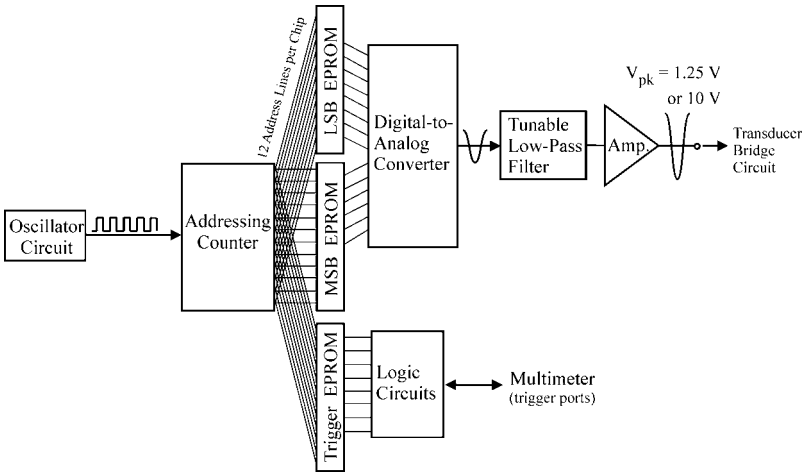

FIG. 9. Functional block diagram of the custom-built frequency generator. The oscillator circuit generates trains of pulses that are counted by the addressing counter. When a pulse is collected by the counter, it sends a binary signal to the top two EPROM chips that "activates" voltages stored in memory cells. A digitized sinusoidal signal is issued from these chips, converted into an analog signal, filtered, and amplified. The bottom EPROM chip triggers a multimeter that measures voltages in loads hooked up to the generator. Up to 512 measurements are taken every cycle, and each voltage measurement by the multimeter is synchronized with the corresponding excitation voltage issued from the EPROM chips.

A. Erasable programmable read-only memory chips and addressing counter

The key components used to generate sinusoidal signals are erasable programmable read-only memory (EPROM) chips. Voltages at even increments of a single cosine cycle with an amplitude of 1 V are stored in consecutive memory cells of two EPROM chips shown in Fig. 9. As explained below, the maximum number of sample voltages that may be used to construct 1 cycle is 4096, and all these voltages are used to generate sinusoidal signals at all frequencies. Since voltages are samplings of a sinusoid at even increments of phase, by outputting these voltages at regular intervals of time, one can generate a sequence of 4096 voltages that sinusoidally vary with time. By sweeping through voltages at a faster rate, a higher-frequency sinusoid is produced.

A voltage value stored in a particular memory cell of an EPROM chip is outputted by feeding into the EPROM a binary signal with the address of the memory cell. Consecutive values of a sinusoid are sequentially stored in memory cells with decimal addresses ranging from 0 to 4095. Therefore, by sending in address signals that step regularly from 0 to 4095, one can sweep through all memory cells and generate a sinusoid. The most practical method of producing such a set of address signals is by counting pulses generated by a digital oscillator circuit (described below), and that is the function of the addressing counter connected to the inputs of the EPROM chips. The counter tallies the number of pulses in pulse trains, and the cumulative count number is outputted by the counter and used as address signals for the EPROM chips. The concept of this operation is illustrated in Fig. 10 for a simpler case where only 11 pulses are required to generate a cycle. In reality, incoming pulse trains contain 4096 pulses, corresponding to the number of addresses that need to be generated each cycle. The figure shows that we control the frequency of sinusoids produced by the EPROM by varying the frequency of pulses, and, in fact, these two frequencies are related to each other by a proportionality factor, $f_{\text{sinusoid}}=f_{\text{pulse}}/4096$. Since the desired frequency range of f_{sinusoid} is 1 mHz–1 kHz, f_{pulse} should range between 4.096 Hz and 4.096 MHz.

The number of sample voltages that may be used to construct 1 cycle is determined by the speed of the EPROM chips. The access time (time required to output data) of the particular chips used in the circuit (M27C256B) is about 100 ns. If 4096 voltages are chosen to be outputted every cycle, the minimum access time required would be $(\text{maximum } f_{\text{pulse}})^{-1}=(4096\times 1\text{ kHz})^{-1}=244$ ns. Since this falls well within the access time limit, outputting 4096 voltages per cycle is a suitable choice. The EPROM chips have the necessary 12 input lines to address 4096 ($=2^{12}$) memory cells; however, each chip has only eight output lines, which gives rather limited resolution of voltages. To improve upon this situation, two EPROM chips are stacked in parallel, and the capacity of each memory cell is expanded to 14 bits, with the six most significant bits of each voltage stored in one chip and the eight least significant bits stored in the other. This permits voltages to be specified with 14 bit resolution ($2^{-14}\cong 60$ ppm).

B. Digital-to-analog converter circuit

The digitized sinusoid (consisting of ministeps) produced by the EPROM chips is converted to an analog signal by digital-to-analog (DAC) chip AD7538KR that is configured for bipolar operation. Since the conversion of this DAC is guaranteed to be monotonic to 14 bits and the differential nonlinearity error of this converter is ± 1 least significant bit,

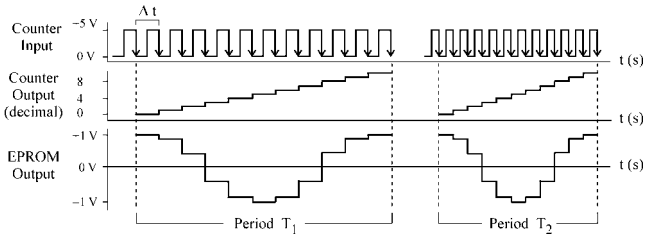

FIG. 10. Illustration of the technique for generating a digital sinusoid. The top line represents pulse trains that are counted by the addressing counter shown in Fig. 9. Sampling time Δt refers to the time interval between pulses (Δt is set between 0.24 μs and 0.24 s). Two sinusoids are represented here (sinusoid frequency is the reciprocal of period T). The output of the counter is the cumulative number of pulses that have entered the counter by a certain time. When this output is used to address memory cells of EPROM chips, a stepwise approximation of a cosine curve is produced. In the simplified cases depicted here, only 11 voltages from a cosine cycle are stored in the EPROM chips; however, in reality, 4096 voltages are stored in the chips.

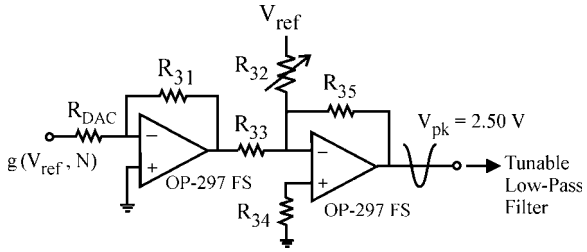

FIG. 11. Equivalent circuit for DAC AD7538KR configured for bipolar operation. Reference voltage V_{ref} is approximately 2.5 V. Adjustable resistor R_{32} has a value near 20 kΩ. $g(V_{ref},N)$ is the Thevenin equivalent voltage generator due to V_{ref} and DAC input code N. The equivalent resistance of the R-$2R$ ladder resistor network in the DAC chip is represented by R_{DAC}, and part of R_{31} depends upon the R value of this network, as well $(R_{31}=22\ \Omega+\frac{1}{4}R)$. The remaining resistors are $R_{33}=10$ kΩ, $R_{34}=5$ kΩ, and $R_{35}=20$ kΩ.

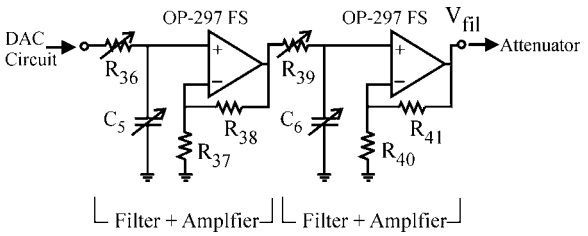

FIG. 12. Low-pass filters and amplifiers. Resistors R_{36} and R_{39} are the same and set to any of the following 16 values (in kΩ): 11.5, 13.3, 15.4, 17.8, 20.5, 23.7, 27.4, 31.6, 36.5, 42.2, 48.7, 56.2, 64.9, 75.0, 86.6, and 100. Capacitors C_5 and C_6 are the same and set to any of the following seven values (in F): 10^{-11}, 10^{-10}, 10^{-9}, 10^{-8}, 10^{-7}, 10^{-6}, and 10^{-5}. Specific values of components are switched in by a microprocessor to give appropriate 3 dB cutoff frequencies for each filter. OP-297FS op-amps are used to isolate the filters. With resistors R_{37}, R_{38}, R_{40}, and R_{41} all equal to 100 kΩ, the amplitude of the signal is doubled by each op-amp.

voltages of the resulting analog signal have at least the same level of accuracy as voltages stored in the EPROM chips. (Once "jaggedness" in the signal produced by digitization is "smoothed out" by low-pass filters described below, absolute errors in the final signal produced by the generator are expected to be smaller than 60 ppm.) Some circuitry based upon operational amplifiers (op-amps) (Fig. 11) is attached to the DAC chip to realize bipolar operation. The output of the first op-amp in the figure is a signal oscillating between about 0 and about −2.5 V, while the second op-amp multiplies this by about −2 and lowers the offset by about 2.5 V to give a signal oscillating between −2.5 and 2.5 V. Voltage V_{ref} (provided by a high precision reference chip AD780 configured with a fine-trim circuit) and resistor R_{32} in Fig. 11 are adjusted so that, when the generator is programed to issue a 10 volt (peak) signal at 10 Hz, the amplitude of the final output signal of the generator meets the desired value within less than 1 mV, and the dc offset is less than 1 mV. This calibration procedure ensures that the 14 bit accuracy of voltages is maintained.

For purposes of measuring bridge circuits containing transducers, absolute errors in voltage matter less than reproducibility errors. [Equation (1) shows that calculations of the transducer impedance depend upon the ratio, V_{gen}/V_{in}. Since V_{gen} and V_{in} occur in the same voltage divider, they are proportional to each other, and, thus, their ratio is not affected if V_{gen} happens to be too large, for example.] A stable output is required to ensure that reference recordings of raw output of the generator remain valid when compared against measurements of transducers that are conducted during a different session. The most significant cause of irreproducibility is temperature drift of key components in the circuit. To estimate the size of this error, the temperature of the DAC circuitry is varied between 20 and 40 °C. It is found that the output voltage varies less than ±1 ppm/°C. Since the temperature sensitivity of this circuit is expected to dominate the overall temperature dependence of the generator's output voltage, we estimate that, if laboratory room temperatures vary by a few °C, the reproducibility error of voltages is no larger than a few parts per million. This result is consistent with our aforementioned measurements of the reproducibility errors of the complex amplitude (V_{gen}) of the overall sinusoid outputted by the generator: in Sec. III, we demonstrated that the reproducibility error of V_{gen} has a ppm order of magnitude.

C. Low-pass filters and amplifiers

Creating a signal from a set of discrete voltages inevitably casts a staircase pattern (as demonstrated in Fig. 10) on the output signal of the DAC circuitry. Since there are actually 4096 steps in each cycle, jumps between steps is reduced from that depicted in the figure; even so, it is important to suppress them further, for voltage steps can cause current spikes in transducers hooked up to the unit, which are typically largely capacitive in nature. To this end, the output signal of the DAC circuitry is directed through a pair of low-pass filters shown in Fig. 12.

In the interest of minimizing possible sources of reproducibility errors, we limit ourselves to using simple RC filters, since filters incorporating coils tend to be much more temperature dependent. (For example, when temperature changes by 20 or 30 °C, impedances of coils typically change by about 1%, primarily due to temperature dependences of their internal resistances; in comparison, capacitors in our filters are on the order of a hundred times less sensitive to temperature changes.) Although RC filters roll off at high frequency more gradually than higher-order filters containing coils, they suffice here since the frequency of steps that we wish to attenuate occurs three decades above the desired signal frequency ($f_{pulse}=4096\times f_{sinusoid}$). A pair of identical RC filters is used to collectively attenuate the step pattern by about 40 dB. To accommodate the range of frequencies generated by the unit, the capacitors can be set to seven possible values (corresponding to the number of available frequency decades), and the resistors can be set to 16 possible values (corresponding to the number of available frequencies per decade, as described below). For example, to smooth out 4.096 MHz steps in a 1 kHz sinusoid, the capacitor and resistor in each filter are set to 10 pF and 11.5 kΩ, respectively, giving a 3 dB cutoff frequency[10] for each filter of $(2\pi RC)^{-1}=159$ kHz. The cascaded filters attenuate the staircase pattern by 98.5%.

Each filter stage is followed by a noninverting op-amp circuit that serves to buffer the filter and double the amplitude of the signal. The output of the second OP-297FS op-

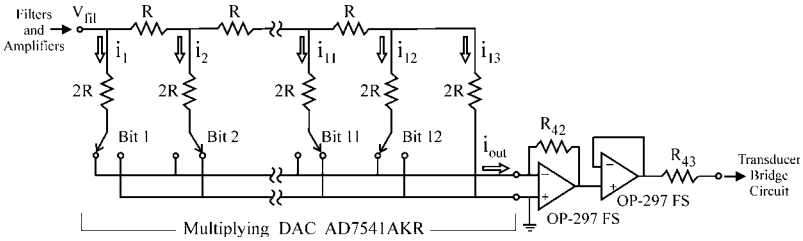

FIG. 13. Programmable attenuator and output buffer amplifier. Multiplying DAC chip AD7541AKR and the OP-297FS op-amp attached to the DAC's output comprise a programmable attenuator. The R-$2R$ ladder of the DAC chip is shown. Switches in the ladder are set by 12 binary input lines. Resistor R is 10 kΩ, and feedback resistor R_{42} is approximately R. The last OP-297FS op-amp serves as an output buffer amplifier. Resistor R_{43} is 4.7 Ω.

amp has an amplitude of 10 V. Often, the optimum amplitude for performing measurements is smaller than this (for example, piezoceramic transducers are excited with a voltage of 1.25 V to minimize nonlinear piezoelectric effects); hence, an attenuator is needed. This is provided in the form of a programmable gain amplifier (with gain less than unity) that is fabricated by using multiplying DAC chip AD7541AKR and another OP-297FS op-amp (Fig. 13). The manner in which the signal is attenuated is straightforward:[11] the DAC functions as a programmable resistor that is used in a simple inverted op-amp circuit. The ratio between the output voltage of the OP-297FS op-amp connected to the DAC and voltage V_{fil} applied to input (reference) port of the DAC is $-R_{42}/R_{\mathrm{eq}}$, where R_{eq} is the equivalent resistance of the DAC between its input (reference) and i_{out} ports. The reduction factor, $-R_{42}/R_{\mathrm{eq}}$, equals $N/2^{12}$, which is a fractional representation of number N encoded on the 12 binary input lines of the DAC chip; hence, not only does this setup allow us to program the reduction factor but also we have the option of specifying it with 12 bit resolution.

The last stage of the generator output is a buffer amplifier, which enables the generator to drive loads as small as 2 kΩ without drawing high currents from the rest of the circuit. A differential amplifier has been added to the output to give us the option of driving 50 Ω loads with peak voltages of 10 V.

D. Oscillator circuit

Since we typically sweep through several frequency decades during a single measurement run, it is convenient to space frequencies evenly apart on a logarithmic scale. We choose 16 frequencies per decade, ranging in magnitude from 1 mHz up to 1 kHz. The frequencies are specified by the formula $f_{\mathrm{sinusoid}}(K,L)=10^{L}\times 10^{K/16}$, with decade index $L=-3,-2,\ldots,2$ and index K equal to an integer lying between 1 and 16 $(10^{K/16}=0.115\,48, 0.133\,35, 0.153\,99, \ldots, 0.749\,89, 0.865\,96, 1.0)$. As pointed out in the above description of the EPROM chips and addressing counter, we control the frequency of sinusoidal signals by setting the frequency of pulses entering the addressing counter. Those pulses are created by an oscillator circuit, which is now described here.

Pulses originate from a voltage-controlled oscillator (VCO) that is included in a phase-locked loop (PLL) chip (Fig. 14).[12] As indicated above (in the description of the EPROM chips and addressing counter), we require pulses with frequencies given by the formula, $f_{\mathrm{pulse}}=4096\times f_{\mathrm{sinusoid}}(K,L)$. The VCO issues pulses with a frequency of about 18 MHz that are then divided down by appropriate factors of N $(f_{\mathrm{pulse}}=f_{\mathrm{VCO}}/N)$ to obtain pulses with the 16 highest frequencies, ranging between 0.473 and 4.096 MHz. These pulse frequencies are used to generate sinusoidal signals with frequencies lying in the highest decade, $100\ \mathrm{Hz} < f_{\mathrm{sinusoid}}(K=1,\ldots,16;L=2) \leqslant 1\ \mathrm{kHz}$. To generate sinusoids with frequencies lying in lower-order decades, these 16 pulse frequencies are divided down by a decade divider, or, for the lowest-order decades $(L=-3,-2,-1)$, by two decade dividers.

If the frequency f_{VCO} of pulses issued by the VCO is fine tuned, it is possible to generate sinusoids with frequencies that closely agree with expected values specified by the K and L indices. This frequency is adjusted by varying the frequency divider placed in the negative feedback loop of the PLL chip. As is conventional with PLL circuits, the phase-frequency detector puts out a corrective voltage to the VCO that changes its output frequency until the signal from the feedback loop matches the phase and frequency of the signal feeding into the reference input of the PLL; hence, $f_{\mathrm{VCO}}=M\times f_{\mathrm{ref}}$. The reference signal is a 2 kHz pulse train that is obtained by dividing down 2.048 MHz pulses produced by a quartz reference oscillator (the Kinseki oscillator in our circuit has a frequency stability of approximately 10 ppm for temperature variations of less than 10 °C near room temperature). Since M is about 9000, frequency f_{VCO} is incremented by about 0.01% when M is increased by one. This degree of selectivity permits us to set the frequency close to a desired value $(f_{\mathrm{VCO}}=f_{\mathrm{pulse}}\times N)$, with discrepancy being

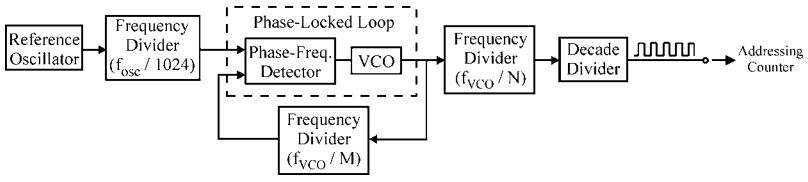

FIG. 14. Functional block diagram of the oscillator circuit that provides pulses for the addressing counter. Frequencies of pulses sent to addressing counter range between 4.73 Hz and 4.096 MHz. The phase-locked loop (TLC2932IPWR) contains an edge-triggered phase-frequency detector and voltage-controlled oscillator (VCO). The reference oscillator is a Kinseki EXO-3C 16.384 MHz that is configured to issue 2.048 MHz pulses. All frequency and decade dividers are 74HC4059D programmable divide-by-n counters.

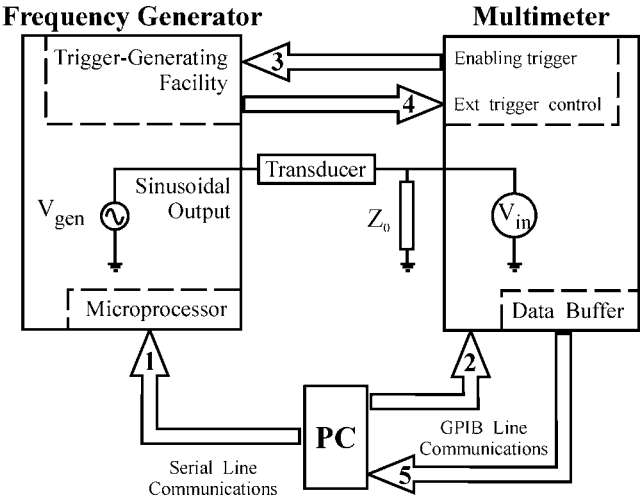

FIG. 15. Schematic of communications among the custom-built frequency generator, multimeter, and personal computer. (1) PC sets frequency parameters in the frequency generator [frequency dividers in the oscillator circuit (Fig. 14) and *RC* low-pass filter (Fig. 12)]. The generator puts out a sinusoidal signal at the chosen frequency. (2) PC sets an integration time in the multimeter, based upon the chosen frequency and the number n of voltage measurements to be performed every cycle (512, for example). (3) When the multimeter is ready to start measurements, it transmits an enabling signal to the triggering facility in the generator. (4) When the generator initiates a new cycle, it starts to transmit data taking triggers to the multimeter. The multimeter makes a measurement every time it receives such a trigger and stores the voltage in a data buffer. (5) After the multimeter makes n measurements in a cycle, the contents of the data buffer are transferred to the PC. However, since initiating excitations at a new frequency introduces start-up transients in the signal, data collected from the first cycle after setting a new frequency are discarded. In fact, the generator is instructed to cycle through three or four times to allow transients to decay away before data are accepted. This setup is used to determine voltage V_{in} during measurements of the transducer. In order to measure voltage V_{gen} during the calibration procedure, the transducer and dummy load Z_0 are replaced by a direct connection between the sinusoidal output of the generator and the voltage input of the multimeter.

only on the order of tens of ppm. The 16 settings of f_{VCO} range between 17.7 and 20.5 MHz.

It is seen that the frequency of pulses issued by this oscillator circuit is determined by settings of the N- and M-frequency dividers and the decade dividers. These dividers are controlled by a microprocessor through a serial communications line. Along with setting the pulse frequency, the microprocessor also selects the *RC* filter (see the above discussion of low-pass filters) appropriate for the sinusoidal frequency that is eventually generated by this pulse frequency. The microprocessor itself receives an instruction from a computer about which sinusoidal frequency to generate. A summary of communications among the computer, frequency generator, and multimeter (discussed below) is given in the caption of Fig. 15.

E. Use of triggers to precisely control timing of voltage measurements

As mentioned above in Sec. III, a bridge circuit is used to measure the electrical impedance (or equivalent complex capacitance) of transducers. Equation (1) shows that our calculation of this impedance depends upon the ratio of voltage V_{gen} outputted by the frequency generator and voltage V_{in} measured across a dummy load (generic plots of these signals are included in Fig. 16). (As indicated in Sec. III, these two voltages are not simultaneously measured.) The complex amplitude of each sinusoidal signal is determined in the following manner:

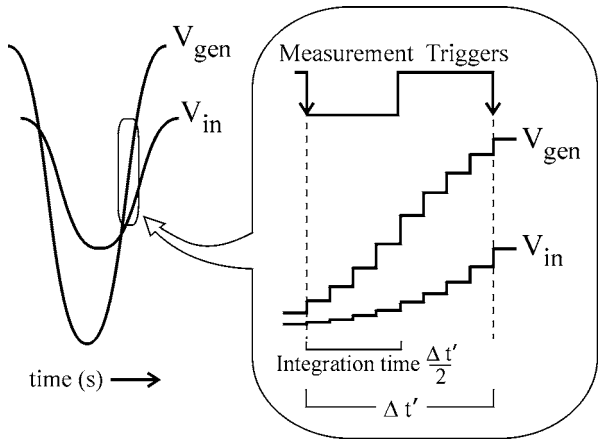

FIG. 16. Generic plots of sinusoidal signal V_{gen} applied to transducer bridge circuit by custom-built frequency generator and sinusoidal signal V_{in} measured across the dummy load in the bridge circuit. Features in the blown-up zone are exaggerated for effect and are not drawn to scale. The staircase patterns in the signals are not realistic and included only to illustrate the time scale of the blown-up graph: the time interval of each step is $\frac{1}{4096}$ of the period of the sinusoidal signal. Two of n (512, for example) triggers issued every cycle to commence measurements of V_{in} are shown in this diagram. $\Delta t'$ is the time interval between measurement triggers, and integration time $\Delta t'/2$ is the period of time during which voltage V_{in} is measured by the multimeter.

(i) The multimeter shown in Fig. 1 measures voltages at n uniform intervals of time in each cycle (typically n is 256 or 512 for reasons explained below).

(ii) Rather than attempting to extrapolate the amplitude and phase of the sinusoid in the time domain, we compute a discrete Fourier transformation of the set using a fast Fourier transform (Cooley–Tukey) algorithm, and we take the coefficient of the first harmonic component as an estimate of the complex amplitude of the sinusoid:

$$V \cong \sum_{m=0}^{n-1} V_m e^{-i2\pi m/n}, \tag{4}$$

where $\{V_m\}$ are measurements of V_{gen} or V_{in} obtained at uniform intervals of time in a single cycle. This approach has the advantage of suppressing effects of high-frequency interference in calculations of V_{gen} and V_{in}, since such interference would tend to affect high-order harmonics, not the first harmonic component.

If measurements of V_{gen} and V_{in} obtained at uniform intervals of time in a single cycle are $\{V_{gen,m}\}$ and $\{V_{in,m}\}$, we have

$$\frac{V_{gen}}{V_{in}} = \frac{\Sigma_{m=0}^{n-1} V_{gen,m} e^{-i2\pi m/n}}{\Sigma_{m=0}^{n-1} V_{in,m} e^{-i2\pi m/n}}. \tag{5}$$

This result is substituted into Eq. (1) to obtain the electrical impedance of the transducer. An error arises if a particular voltage $V_{gen,m}$ or $V_{in,m}$ is not measured at the same interval of time as the rest of the voltages; in the formula above, this

error would be manifest as an extra phase factor that would appear in the term containing the particular voltage. Thus, it is critical that measurements occur at regular intervals of time.

Rather than relying upon the multimeter's internal clock to perform this crucial timing (the reliability of which depends upon its state of calibration), we resort to a timing method that employs the high precision of the oscillator circuit in the frequency generator. The same digital pulses that establish the precise time base for the generator can be used to control the timing of measurements by the multimeter, as well. As described in more detail below, measurements are externally triggered by pulses that are resolvable on the same time scale as pulses issued by the oscillator. Since the oscillator issues 4096 pulses/cycle, the timing of a pulse is guaranteed to be precise to at least within $2\pi/4096 \cong 0.0015$ rad. In fact, most voltages in the sets $\{V_{\mathrm{gen},m}\}$ and $\{V_{\mathrm{in},m}\}$ have timing errors that are smaller than 0.0015 rad; for our aforementioned measurements of complex amplitude V_{gen} (see Sec. III) indicate that reproducibility error of the phase of V_{gen} is approximately 1 ppm $[=\mathrm{Im}(\delta V_{\mathrm{gen}}/V_{\mathrm{gen}})]$, and this implies that most timing errors of voltages $\{V_{\mathrm{gen},m}\}$ do not exceed 10^{-6} rad. Another consideration is that any systematic errors in timings of measurements of $\{V_{\mathrm{gen},m}\}$ and $\{V_{\mathrm{in},m}\}$ are partially canceled when the ratio $V_{\mathrm{gen}}/V_{\mathrm{in}}$ is calculated. Any extra phase factors that appear in terms of the numerator of Eq. (5) also appear in corresponding terms in the denominator, and effects of any errors are ameliorated somewhat. As an extreme example, even if every term in the numerator were shifted in phase by the same phase factor, the phase angle of the ratio of Eq. (5) would not be affected since every term in the denominator would also be affected by the same phase factor.

A key aspect of this setup is that the frequency generator is able to send multiple trigger signals to the multimeter every cycle. This is not an available option with most conventional frequency generators. Commercial units typically send triggers only at the beginning of the cycle, not at points throughout the cycle. The unique triggering facilities of this unit are centered at an EPROM chip, which is described below.

For purposes of making precise determinations of complex amplitudes V_{gen} and V_{in}, the number of measurements made per cycle, n, should be as large as practical. The upper limit of n depends upon the frequency of the sinusoidal signals and the resolution at which we wish to measure voltages. As mentioned above, we are keenly interested in the reproducibility of signals. In order to monitor reproducibility errors, which are expected to be on the order of parts per million, we require 18 bit resolution in our voltage measurements. This level of resolution can be achieved if a signal is sampled over a sufficiently long window of time. This time window, called the integration or aperture time, refers, for example, to the period of time over which a capacitor in a sample-and-hold circuit is charged. The capacitor integrates the input voltage, and the multimeter reads the voltage averaged over the integration time. The longer this time interval is, the more that high-frequency noise is averaged out. When the multimeter is set in high speed, dc voltage sampling mode with external triggering, 18 bit resolution is obtained if the integration time is at least 10 μs. If another 10 μs is allocated for transferring and processing data, measurements can be taken no more frequently than once per 20 μs. If the maximum frequency of sinusoids that are measured using the multimeter is the last one in the sequence below 100 Hz (86.596 Hz, to be precise) then the maximum number of voltages that can be measured per cycle at this frequency is $[(86.596\ \mathrm{Hz})\ (20\ \mu\mathrm{s})]^{-1}=577$. For convenience, as explained below, we typically choose 512 measurements/cycle. We maintain this number for measurements at lower frequencies, and that permits us to extend the integration time beyond the minimum of 10 μs, which aids the accuracy and resolution of measurements. As shown in Fig. 16, we set the integration time to half the time interval between measurement triggers. Prior to commencing measurements at a new frequency, a command is sent from the PC to the multimeter to change the integration time (as indicated in Fig. 15).

F. Source of triggers: Third EPROM chip

We wish to provide trigger signals that are precisely timed by pulses issued from the oscillator circuit. The most practical way to accomplish this is by, once again, exploiting the idea of issuing voltages stored on an EPROM chip at a rate dictated by the pulse frequency. Voltages for trigger signals at six different frequencies are stored on the third EPROM chip shown in Fig. 9, and they are outputted by the same address signals that output sinusoidal voltages stored in the other two chips. This arrangement ensures that trigger signals are always synchronized with voltages outputted from the generator, as would be expected of triggers. More significantly, since addressing signals jump from one value to the next at the rate at which pulses enter the addressing counter, triggering pulses possess the same resolution in timing as pulses issued from the oscillator, which is our chief goal.

As described above, we require trigger signals to be issued at n uniform intervals of time in each cycle. With timing of our triggers based upon oscillator pulses, and with 4096 $(=2^{12})$ pulses making up 1 cycle, we find it most convenient to choose a power of 2 for n: typically, n is set to 512, but we also have the option of setting it to 256, 128, 64, 32, or 16. Equivalently, trigger signals are issued every 8, 16, 32, 64, 128, or 256 pulses. Separate output lines of the third EPROM chip are reserved for six trigger signals, and we select the trigger signal that is outputted from the generator by manually setting a switch. Figure 16 shows the shape of the trigger signal that is issued for the case, $n=512$. An edge trigger occurs every eight steps, corresponding to once per eight addresses received by the EPROM chip.

With this apparatus for issuing triggering signals in place, measurements over the course of 1 cycle could proceed, in principle, as follows. The PC would send an enabling signal to logic circuits (shown in Fig. 9) governing the outflow of triggering signals to the multimeter. This enabling signal by itself would not initiate triggering of the multimeter since we do not want to start measurements until the genera-

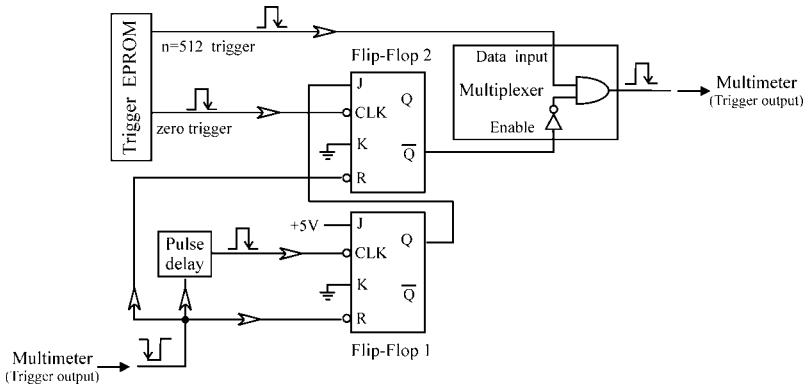

FIG. 17. Logic circuit governing the outflow of triggering signals sent from the trigger EPROM to the multimeter. For the sake of simplicity, only two of the eight output lines of the trigger EPROM are shown. The pulse delay is a monostable multivibrator 74HC221 chip. A high-to-low edge input triggers a high-level output pulse with a width set by external resistor R_{ext} $=100\ \mathrm{k}\Omega$ and external capacitor $C_{ext}=0.22\ \mu\mathrm{F}$ (duration of pulse$=0.7\ R_{ext}\ C_{ext}=15$ ms). The *J-K* flip-flops are 74HC73 chips with high-to-low, edge-triggered clock inputs and asynchronous reset inputs (activated when low). The multiplexer is a 74HC153 chip that basically functions as a logical AND gate.

tor starts to output a new cycle (when V_{gen} is at the top of a cosine curve). No triggers would be permitted to flow beyond the logic circuit until decimal address 0 is delivered to the EPROM chips by the addressing counter, initiating output of a new cycle from the EPROM chips. When this occurs, a special trigger (referred to here as the "zero trigger") would be issued through a separate output line of the trigger EPROM to the logic circuits, opening up its output. At this point, triggering signals would be sent to the multimeter, and measurements would commence after a delay of 165–175 ns. In reality, the situation is slightly more complicated than this since the enabling signal for the logic circuits does not come directly from the PC but rather is routed through the multimeter. The rationale behind doing this is that the multimeter needs to carry out preparations before measurements should commence. For example, a zero compensation operation needs to be performed, whereby input ports to the multimeter are momentarily shorted out to avoid voltage drift. Also, before initiating a measurement at a new frequency, a new integration time must be set (as mentioned above in the discussion of the measurement triggers). The last step is setting the multimeter in external-triggering mode. Since the enabling signal must be forwarded to the logic circuits shortly before this occurs, it is necessary to include a pulse delay in the logic circuits, so that triggers are not prematurely sent to the multimeter before it has had a chance to slip into external-triggering mode.

Details of these logic circuits regulating triggers sent from the EPROM to the multimeter are shown in Fig. 17. Upon arrival at the logic circuits, the 1 μs long, low-going enabling signal from the multimeter pulse immediately resets both flip-flops. In particular, the complementary output of flip-flop 2 switches to high, and this disables the multiplexer, preventing any further triggers (perhaps for a preceding measurement done at a different frequency) from reaching the multimeter. The monostable vibrator serves the function of providing the aforementioned delay required for the multimeter to properly set itself up (a delay of 15 ms is adequate). The two flip-flops are needed to solve a common problem encountered with asynchronous communications; namely, can one predict what will happen if, by coincidence, the delayed enabling signal overlaps the zero trigger transmitted from the EPROM chip when they arrive at the logic gates? With the arrangement shown, potential timing conflicts are avoided by converting one edge trigger into a level. The low-going edge input of the delayed enabling signal causes the Q output of flip-flop 1 to become high and hold at that level. Since the J input of flip-flop 2 is held high, too, the low-going edge input of the zero trigger will cause the complementary output of this flip-flop to become low and hold at that level. This will enable the multiplexer and allow triggers from the EPROM to be transmitted to the multimeter. If, by chance, the low-going edge input of the zero trigger arrives at flip-flop 2 shortly before the J input has been changed to high, the output will not toggle, and the multiplexer will remain disabled. This is not a worrisome situation for great concern, though; when the next zero trigger is transmitted after a wait of 1 cycle, the output will change and the multiplexer will become enabled.

V. FUTURE IMPROVEMENTS OF EQUIPMENT

(*1*) *Stabilized output of the custom-built frequency generator*. As noted in Sec. III, the output voltage of the custom-built frequency generator has a reproducibility error of only about 1 ppm when measurements are taken over the time span of a day, but, for longer periods of time, the output drifts, possibly due to changes of temperature of the unit's output circuitry. We propose stabilizing this temperature by encasing critical components in a metal box and mounting it on a Peltier element. In addition, we are considering ways to stabilize the temperature of the entire laboratory room, which would enhance the stability of all electronic circuits in our setup.

(*2*) *Increased accuracy of voltages produced by the custom-built frequency generator*. As described in Sec. IV A, signals produced by the custom-built frequency generator originate from voltages stored on a pair of memory chips, each with an 8 bit output (see Fig. 9). We use 14 of the 16 available output bits to transmit voltage at a single point of a sinusoid, which allows us to specify voltages with an accuracy of about 60 ppm. The output is currently restricted to 14 bits because the signal feeds into a DAC with 14 input bits (see Sec. IV A); however, if we replace this DAC with a 16 bit model, we will be able to take advantage the full capacity of the memory chips. The accuracy of stored voltages will improve by a factor of 4, to approximately 15 ppm.

(*3*) *Software-selectable number of triggers issued by the frequency generator*. As described in Sec. IV E, a triggering facility in the frequency generator controls the timing of measurements by the multimeter. The multimeter records n voltages per cycle that are evenly spaced apart in phase, and,

currently, we use a single setting of n (16, 32, 64, 128, 256, or 512, as set by a manually operated switch) for all frequencies outputted by the frequency generator during a data-collecting session. If we had the option to automatically drop n to a lower setting for higher frequencies, though, it would be possible to extend the range of operating frequencies above 100 Hz. As explained in Sec. IV E, the maximum allowable frequency is determined by the constraint that measurements can be performed no more frequently than once per 20 μs if we wish to measure voltages with ppm precision. When n is set to 512, this upper limit is 98 Hz, but, if we program n to switch to a lower value as we approach this frequency, we could run the generator at several hundred hertz or even a few kilohertz.

(*4*) *Improved LCR meter*. As indicated in Sec. II, we are in the process of replacing the Agilent 4284A *LCR* meter described in this setup with another model, Agilent E4980A, which is capable of measuring impedance (capacitance) at more frequencies in the upper frequency ranges. This will obviate the need to switch to the HP 4192A impedance analyzer to make measurements above a few multiples of 10 kHz. Aside from yielding the benefit of simplified measuring procedures, this modification will enable us to make more precise measurements in these upper frequency ranges since, as pointed out in Sec. II, the precision of the *LCR* meter is slightly better than that of the impedance analyzer.

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